

Model Predictive Control of Quasi-Z-Source Four-Leg Inverter

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Abstract—This paper presents a model predictive control (MPC) scheme for quasi-Z-source (qZS) three-phase fourleg inverter. In order to cope with the drawbacks of traditional voltage source inverters (VSIs), a qZS three-phase four-leg inverter topology is proposed. This topology features a wide range of voltage gain which is suitable for applications in renewable energy-based power systems, where the output of the renewable energy sources varies widely with operating conditions such as wind speed, temperature, and solar irradiation. To improve the capability of the controller, an MPC scheme is used which implements a discrete-time model of the system. The controller handles each phase current independently, which adds flexibility to the system. Simulation and experimental studies verify the performances of the proposed control strategy under balanced and unbalanced load conditions as well as single-phase open-circuit fault condition.

Index Terms—DC-AC power conversion, four-leg inverter, model predictive control (MPC), quasi-Z-source inverter (qZSI).

I. INTRODUCTION

NCREASINGenvironmental awareness as a consequence of climate change and the exhaustible nature of fossil fuels have increased the importance of renewable energy sources (RESs). However, interconnecting renewable energy generation into the electrical distribution systems require power electronics to generate and condition the electrical power to meet voltage and frequency specifications. The performance of these renewable energy systems thus depends on the power converter topology and control method [1]. In most cases, such systems use

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three-phase voltage-source inverter (VSI) to supply the power to either the grid or the local loads. This approach is straightforward to implement, but suffers from two major drawbacks: 1) input voltage variation and 2) unbalanced output current.

The first drawback is the variation in the input voltage due to intermittent and stochastic nature of RES. The VSI must have an input voltage that is greater than the maximum value of the line-to-line output voltage in order to guarantee reliable and uninterruptible power for the loads, which is a major challenge in such systems. To overcome this, dc/dc boost converter is often used as an input stage to create a well-regulated voltage for the VSI. However, this solution results in complex power circuit and multiloop control structure which leads to lower reliability and higher cost. The alternative topology to VSI is a current-source inverter (CSI), which has the advantage of voltage boosting capability without using dc-dc boost converter [2]. This results in less complexity of the system and its control. However, CSI has some drawbacks as follows. 1) Its output voltage cannot be lower than the dc input voltage. 2) Overlap time between phase legs is required to avoid the open circuit of all upper switching devices or all lower devices. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. Furthermore, overlap time for safe current commutation is needed in the CSI, which causes waveform degradation [3]. Recently, a number of new power converter topologies have been proposed to cope with these problems [4]. The quasi-impedance source inverter (qZSI) can overcome the aforementioned problems [5], [6]. They advantageously utilize the shoot-through of the inverter bridge to boost voltage in the VSI (or open circuit in the CSI to buck voltage). Thus, buck-boost functionality is achieved with a single-stage power conversion with a simple L–C network [7].

A second drawback of three-phase VSI topology is that these inverters are usually designed for balanced three-phase loads. However, unbalanced load conditions are common in distribution power generation system where power is delivered to local loads. Unbalanced load condition creates unbalanced current circulating in the power system, causing overheat of the neutral line and harmonic distortion on the output voltage [8], [9]. One way to alleviate this condition is to use a three-phase four-leg VSI. This topology can produce balanced three-phase output even when the load is unbalanced and nonlinear, making it a good choice for standalone power generation and three-phase UPS systems [10].

The control strategy of the power converter plays a crucial role to ensure reliable and efficient operation of the renewable energy-based power generation systems. There are a number of proposed control strategies for the qZSI [11]–[17]. Methods for three-phase four-leg VSI have also been studied [18], [19]. In most applications, proportional-integral (PI)-based cascade control structure has been employed to control current, voltage, etc. [20]. Although this control technique is easy to implement, it has some drawbacks. The major drawback is that the performance of the entire system depends on the performance of the inner control loop [21]. This controller requires a modulator, such as 3-D-SVPWM, to generate PWM signals for the power switches to implement the desired control action.

The model predictive control (MPC) is an attractive alternative to the classical control methods due to its fast dynamic response, simple concept, and ability to include different nonlinearities and constraints [22]. The major advantage of MPC lies in the direct application of the control action to the converter, without requiring a modulation stage. Several studies have been presented under the name of MPC for current control of traditional three-phase inverter [23], multilevel inverters [24]–[27], qZSI [28], and several electrical machine drives [29]–[32]. It is concluded that MPC is currently one of the most attractive control techniques for power converters and machine drives.

This paper presents MPC strategy of quasi-Z-source (qZS) three-phase four-leg inverter. As a response to the gaps in this research area, the contributions of this study are summarized as follows.

- qZS network has been used instead of a dc-dc+dc-ac converter to overcome the drawbacks of traditional threephase VSI topology and two-stage power conversion.
- 2) A three-phase four-leg inverter has been employed to ensure reliable operation of renewable energy-based power generation system under balanced and unbalanced load conditions.
- 3) MPC is used to control load current and qZS network capacitor voltage with high accuracy and fast response.
- 4) The proposed controller handles each phase current independently. As a result of this, the proposed qZS four-leg inverter provides fault-tolerant capability, e.g., if one leg fails, the other can work normally.

In order to verify the steady-state and transient-state performances of the proposed control method, simulation and experimental studies were carried out with different operating conditions. This paper is organized as follows. An overview of the proposed topology and the mathematical model are presented in Section II. The proposed MPC strategy is described in Section III. In Section IV, simulation and experimental results are presented for different operating conditions. Finally, the conclusion is provided in Section V.

II. QZS FOUR LEG INVERTER MODEL

A. Topology

The qZS four-leg inverter topology with R-L output filter is shown in Fig. 1. This topology can be investigated as two stages: 1) the qZS network and 2) four-leg inverter with R-L output filter and load.

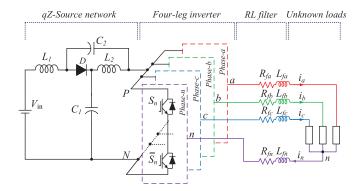


Fig. 1. qZS three-phase four-leg inverter topology.

In the first stage of this topology, the qZS is made of an $L\!-\!C$ impedance network, which can boost the dc voltage in response to the so-called shoot-through zero state of the inverter switching cycle. In the shoot-through zero state, two semiconductor switches in the same leg are simultaneously switched on to create short-circuit across the dc link. During this state, energy is transferred in the qZS network from the capacitors to the inductors, and this state is used to boost the dc voltage.

In the second stage of this topology, the four-leg inverter is used. As shown in Fig. 1, the load neutral point is connected to the mid-point of the inverter's fourth phase leg to allow for zero sequence current/voltage. However, the addition of an extra leg makes the switching schemes more complicated compared to a three-leg VSI. Nevertheless, using the extra phase leg improves inverter capability and reliability. The four-leg inverter can be used under balanced/unbalanced and/or linear/nonlinear load conditions.

B. Mathematical Model of the qZS Network

The equivalent circuits of the qZS network in nonshoot-through and shoot-through states are illustrated in Fig. 2(a) and (b), respectively [33]. All voltages and currents are defined in this figure and the polarities are shown with arrows.

1) Nonshoot-Through State: During the nonshoot-through state, four-leg inverter model is represented by a constant current source; it can be seen from Fig. 2(a). By applying Kirchhoff's voltage law to Fig. 2(a), inductor voltages $(v_{L1} \text{ and } v_{L2})$, dc-link voltage (v_{PN}) , and diode voltage (v_{diode}) are written as

$$v_{L1} = V_{\rm in} - V_{C1}, \quad v_{L2} = -V_{C2}$$
 (1)

$$v_{\rm PN} = V_{C1} - v_{L2} = V_{C1} + V_{C2}, \quad v_{\rm diode} = 0.$$
 (2)

2) Shoot-Through State: During the shoot-through state, four-leg inverter model is represented by short-circuit, it can be seen from Fig. 2(b). By applying Kirchhoff's voltage law to Fig. 2(b), inductors voltages $(v_{L1} \text{ and } v_{L2})$, dc-link voltage (v_{PN}) , and diode voltage (v_{diode}) are written as

$$v_{L1} = V_{C2} + V_{\text{in}}, \quad v_{L2} = V_{C1}$$
 (3)

$$v_{\rm PN} = 0, \quad v_{\rm diode} = V_{C1} + V_{C2}.$$
 (4)

At steady state, the average voltage of the capacitors over one switching cycle are

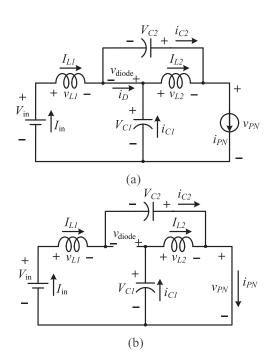


Fig. 2. Equivalent circuit of the qZS network. (a) In nonshoot-through state. (b) In shoot-through state.

$$V_{C1} = \frac{T_1}{T_1 - T_0} V_{\text{in}}$$

$$V_{C2} = \frac{T_1}{T_1 - T_0} V_{\text{in}}$$
(5)

where T_0 is the duration of the shoot-through state, T_1 is the duration of the nonshoot-through state, and $V_{\rm in}$ is the input dc voltage.

From (2), (4), and (5), the peak dc-link voltage across the inverter bridge in Fig. 1 is

$$v_{\rm PN} = V_{C1} + V_{C2} = \frac{T}{T_1 - T_0} V_{\rm in} = BV_{\rm in}$$
 (6)

where T is the switching cycle $(T_0 + T_1)$ and B is the boost factor of the qZSI. The average current of the inductors L_1 and L_2 can be calculated from the system power P

$$I_{L1} = I_{L2} = I_{\rm in} = P/V_{\rm in}.$$
 (7)

Applying Kirchhoff's current law and (7) results in

$$i_{c1} = i_{c2} = i_{PN} - I_{L1}.$$
 (8)

The voltage gain (G) of the qZSI can be expressed as

$$G = \hat{v}_{\rm ln}/0.5v_{\rm PN} = MB \tag{9}$$

where M is the modulation index and \hat{v}_{\ln} is the peak ac-phase voltage.

C. Mathematical Model of the Four-Leg Inverter

The equivalent circuit of the four-leg inverter with the output R-L filter is shown in Fig. 3, where the L_{fj} is the filter inductance, R_{fj} is the filter resistance, and R_j is the load resistance for each of the phase j=a,b,c.

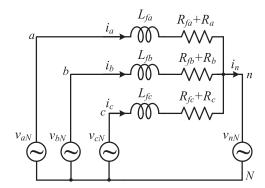


Fig. 3. Equivalent circuit of the three-phase four-leg inverter.

For a three-phase four-leg inverter, the addition of the fourth leg makes the switching states $16 (2^4)$. The valid switching states with the corresponding phase and line voltages for the traditional four-leg inverter are presented in [34]. In addition to these switching states, for this application, one extra switching state is required in order to ensure shoot-through state. Therefore, a total of 17 switching states are used in this application.

The voltage in each leg of the four-leg inverter can be expressed as

$$\begin{cases}
v_{aN} = S_a v_{dc} \\
v_{bN} = S_b v_{dc} \\
v_{cN} = S_c v_{dc} \\
v_{nN} = S_n v_{dc}
\end{cases}$$
(10)

where S_a , S_b , S_c , and S_n are the switching states, and $v_{\rm dc}$ and v_{nN} are dc link and load neutral voltages, respectively.

The output voltage of this inverter can be written in terms of the previous inverter voltages

$$\begin{cases}
 v_{an} = (S_a - S_n)v_{dc} \\
 v_{bn} = (S_b - S_n)v_{dc} \\
 v_{cn} = (S_c - S_n)v_{dc}.
 \end{cases}$$
(11)

By applying Kirchhoff's voltage law to Fig. 3, the inverter voltages can be expressed in terms of load-neutral voltages and load currents as follows:

$$\begin{cases}
 v_{aN} = (R_{fa} + R_a) i_a + L_{fa} \frac{di_a}{dt} + v_{nN} \\
 v_{bN} = (R_{fb} + R_b) i_b + L_{fb} \frac{di_b}{dt} + v_{nN} \\
 v_{cN} = (R_{fc} + R_c) i_c + L_{fc} \frac{di_c}{dt} + v_{nN}.
 \end{cases}$$
(12)

From (11) and (12), the output voltages can be expressed as

$$v_{an} = (R_{fa} + R_a) i_a + L_{fa} \frac{di_a}{dt}$$

$$v_{bn} = (R_{fb} + R_b) i_b + L_{fb} \frac{di_b}{dt}$$

$$v_{cn} = (R_{fc} + R_c) i_c + L_{fc} \frac{di_c}{dt}$$
(13)

which is simplified to

$$v_j = (R_{fj} + R_j) i_j + L_{fj} \frac{di_j}{dt}, \quad j = a, b, c$$
 (14)

and neutral current i_n can be written as

$$i_n = i_a + i_b + i_c.$$
 (15)

The expression for output current, derived from (14), is

$$\frac{di_j}{dt} = \frac{1}{L_f} \left[v_j - (R_{fj} + R_j) i_j \right], \quad j = a, b, c.$$
 (16)

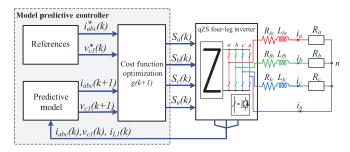


Fig. 4. Block diagram of the proposed MPC scheme.

III. PROPOSED MPC

The proposed MPC scheme is shown in Fig. 4. It has two main layers: 1) a predictive model and 2) cost function optimization. The discrete-time model of the system is used to predict future behavior of the control variables. The cost function is used to minimize the error between the reference and the predicted control variables in the next sampling time. This control technique has several advantages as follows: easy to implement in both linear and nonlinear systems, it shows high accuracy and fast dynamic response, and it has very small steady-state error throughout different operating points. More detailed analysis of the MPC technique and its characteristics can be found in [35]. Here, the proposed MPC scheme is described in the following steps:

- 1) determination of references;
- 2) build discrete-time models of the system;
- 3) define a cost function *g*;
- 4) prepare control algorithm.

A. Determination of References

DC-link voltage and output currents references are normally obtained through maximum power point tracking algorithm for RESs. However, the objective of this paper is the control capability of the qZS four-leg inverter. For this reason, without loss of generality, these references are left to be defined by the user.

B. Discrete-Time Models of the System

The control of the qZS four-leg inverter output currents (i_a, i_b, i_c) and capacitor voltage (V_{C1}) required two discrete-time models be created from the continuous-time equations. To do that, the general structure of the forward-difference Euler equation (17) is used so as to compute the differential equations of the output current and the capacitor voltage

$$\frac{df}{dt} \approx \frac{f(x_0 + h) - f(x_0)}{h}. (17)$$

To estimate the value in the next sample time, for a suitably small time step, (17) becomes the discretization equation

$$\frac{\Delta f(k)}{\Delta t} \approx \frac{f(k+1) - f(k)}{T_s} \tag{18}$$

where T_s is the sampling time.

1) Predictive Model 1: This model is used to predict future behavior of each of the output currents (i_a, i_b, i_c) . The continuous-time expression for each phase current is given in (16). By substituting (18) into (16), the discrete-time model for each output phase current is

$$i_j(k+1) = A_v v_j(k+1) + A_i i_j(k), \quad j = a, b, c$$
 (19)

where $i_j(k+1)$ is the predicted output current vector at the next sampling time and A_v and A_i are constants as defined by

$$A_{v} = \frac{T_{s}}{L_{f} + (R + R_{f})T_{s}}$$

$$A_{i} = \frac{L_{f}}{L_{f} + (R + R_{f})T_{s}}.$$
(20)

2) Predictive Model II: This model is used to predict future behavior of the capacitor voltage (V_{C1}) . The continuous-time model of the capacitor current can be expressed as

$$i_{C1} = C_1 \frac{d(V_{C1} - i_{C1}r_c)}{dt}$$
 (21)

where C_1 and r_c are the capacitance and the equivalent series resistance (ESR) of the capacitor, respectively. Based on (21), the capacitor voltage is derived as

$$\frac{dV_{C1}}{dt} = r_c \frac{di_{C1}}{dt} + \frac{1}{C_1} i_{C1}.$$
 (22)

By substituting (18) into (22), the discrete-time model of the V_{C1} can be obtained as

$$V_{C1}(k+1) = V_{C1}(k) + i_{C1}(k+1)r_c + i_{C1}(k)\left(\frac{T_s}{C} - r_c\right)$$
(23)

where $V_{C1}(k+1)$ is the predicted capacitor voltage at the next sampling time and $i_{C1}(k)$ is capacitor current that depends on the states of the qZSI topology. According to the operational principle of qZS network explained in Section II-B, for nonshoot-through and shoot-through states, capacitor current can be defined as follows:

1) during nonshoot-through state

$$i_{C1} = I_{L1} - (S_a i_a + S_b i_b + S_c i_c) \tag{24}$$

2) during shoot-through state

$$i_{C1} = -I_{L1}. (25)$$

C. Cost Function Optimization

The selection of the cost function is a key part of the MPC scheme. The proposed MPC scheme has two cost functions, which are used to minimize output current and capacitor voltage errors in the next sampling time. The output current cost function is defined as

$$g_{i} = \|\mathbf{i}_{j}^{*}(k+1) - \mathbf{i}_{j}(k+1)\|^{2}$$

$$= [i_{a}^{*}(k+1) - i_{a}(k+1)]^{2}$$

$$+ [i_{b}^{*}(k+1) - i_{b}(k+1)]^{2}$$

$$+ [i_{c}^{*}(k+1) - i_{c}(k+1)]^{2}$$
(26)

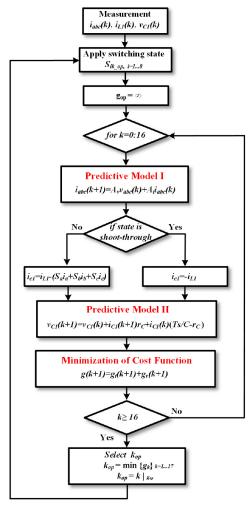


Fig. 5. Flowchart of the proposed MPC algorithm for qZS four-leg inverters.

where $i_j^*(k+1)$ is the reference output current vector and $i_j(k+1)$ is the predicted output current vector in the next step (j=a,b,c).

The cost function of capacitor voltage can also be defined as

$$g_v = \lambda * |v_{C1}^*(k+1) - v_{C1}(k+1)| \tag{27}$$

where $v_{C1}^*(k+1)$ and $v_{C1}(k+1)$ are the reference and predicted capacitor voltages, respectively. The weighting factor (λ) was determined by using cost function classification technique that was detailed in [36]. The complete cost function is

$$g(k+1) = g_i(k+1) + g_v(k+1).$$
 (28)

D. Control Algorithm

The flowchart for the proposed control algorithm is given in Fig. 5. Cost function minimization is implemented as a repeated loop for each voltage vector to predict the values, evaluate the cost function, and store the minimum value and the index value of the corresponding switching state. The control algorithm can be summarized in the next steps.

1) Sampling the output phase currents (i_{abc}) , inductor current (i_{L1}) , and capacitor voltage (v_{C1}) .

TABLE I

QZS FOUR-LEG INVERTER AND LOAD PARAMETERS

Parameter	Value
Input dc voltage (V_{in})	80–180 V
qZS network inductances (L_1, L_2)	2.5 mH
qZS network capacitors (C_1, C_2)	$1000~\mu F$
Load resistance	$5-10 \Omega$
Filter inductance, L_f	10 mH
Filter resistance R_f	$0.05~\Omega$
Nominal frequency (f_o)	50 Hz
Nominal output voltage (v_{ln})	50 V rms
Sampling time (T_s)	$40~\mu s$

- These are used to predict output currents and capacitor voltage using the predictive model I, and II, respectively.
- 3) All predictions are evaluated using the cost function.
- 4) The optimal switching state that corresponds to the optimal voltage vector that minimizes the cost function is selected to be applied at the next sampling time.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the theoretical analysis and confirm the proposed MPC technique of qZS four-leg inverter, simulation and experiments have been conducted with the configuration shown in Fig. 1. The parameters for both simulation and experiments are given in Table I.

A. Buck-Boost Conversion Modes Analysis

The proposed qZS four-leg inverter can operate both buck and boost conversion modes according to the input voltage and the desired output voltage. To test voltage gain and boost factor performances of the four-leg qZSI, the input voltage is changed from 180 to 80 V. To simplify the analysis, we assume that the output voltage $(v_{\rm ln})$ is equal to the load voltage (v_R) and the voltage on R-L filter is neglected. In order to ensure the same load voltage $(\hat{v}_{\rm ln}=50\cdot\sqrt{2})$ at wide range input voltage, the reference output currents are $(i_a^*=i_b^*=i_c^*)$ set to 7 A and loads are balanced $(R_a=R_b=R_c=10~\Omega)$.

The minimum input voltage must be $V_{\rm in}=2\hat{v}_{\rm ln}/M=123~{\rm V}$ (with $M=2/\sqrt{3}$) to maintain 50 V rms output voltage. If the input voltage is above 123 V, the qZSI can operate in buck conversion mode; whereas, if it is below 123 V, the qZSI can operate in boost conversion mode.

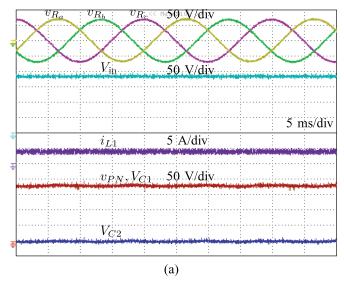
Case-A1: $V_{\rm in} = 180 \text{ V}, M = 0.8.$

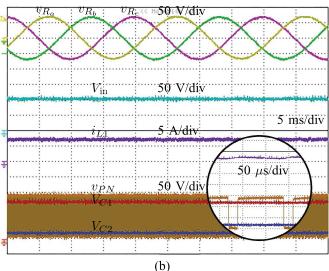
Experimental results of this case are shown in Fig. 6(a). Here, $V_{\rm in}>123$ V, so qZSI works in buck conversion mode. Thus, the boost factor B=1 and the voltage gain is $G=B\cdot M=0.8$. The maximum output line-to-line voltage is

$$\hat{v}_{ab} = \hat{v}_{bc} = \hat{v}_{ca} = \sqrt{3} \cdot G \cdot V_{in}/2 \cong 123 \text{ V}.$$

It can be observed from Fig. 6(a) that the voltage on C_1 is equal to the input voltage 180 V and the voltage on C_2 is 0 V. It can be noted that a pure dc current flows through an inductor due to the voltage on L_1 is zero.

Case-A2:
$$V_{\rm in} = 100 \text{ V}, M = 1.$$





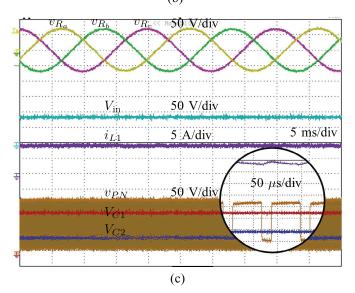


Fig. 6. Experimental results with the same output voltage at (a) $V_{\rm in}$ =180 V, M=0.8; (b) $V_{\rm in}=100$ V, M=1; and (c) $V_{\rm in}=80$ V, M=0.85.

In order to maintain constant output voltage, qZSI works in boost conversion mode because of $V_{\rm in}$ <123 V. From (9), one can get the boost factor $B\cong 1.42$ and the voltage gain $G\cong 1.42$. The experimental results of this test are shown in Fig. 6(b). The voltage on the dc link $(v_{\rm PN})$ is boosted from 100 to 142 V. In this case, the maximum output line-to-line voltage is

$$\hat{v}_{ab} = \hat{v}_{bc} = \hat{v}_{ca} = \sqrt{3} \cdot G \cdot V_{in}/2 \cong 123 \text{ V}.$$

It can be seen from Fig. 6(b) that the voltage on C_1 and C_2 is 120 and 22 V, respectively. Notice that the inductor current (i_{L1}) is continuous that reduce the input stress.

Case-A3: $V_{\rm in} = 80 \text{ V}, M = 0.85.$

Fig. 6(c) shows the experimental results for this case. From (9), the boost factor B=2.08 and the voltage gain G=1.768 is obtained. Thus, the dc-link voltage $(v_{\rm PN})$ is boosted from 80 to 166 V. In this case, the maximum output line-to-line voltage is

$$\hat{v}_{ab} = \hat{v}_{bc} = \hat{v}_{ca} = \sqrt{3} \cdot G \cdot V_{in}/2 \cong 123 \text{ V}.$$

It can be seen from Fig. 6(c) that the voltage on C_1 and C_2 is 124 and 42 V, respectively. Experimental results show that the qZS four-leg inverter can provide constant output voltage under various input voltages without using dc/dc converter or transformer.

B. Steady-State Analysis

To perform steady-state analysis, the reference of qZS network capacitor voltage (V_{c1}^*) is set to 150 V and the input voltage is $V_{\rm in}$ =100 V, which results in the qZS four-leg inverter operating in boost mode in the following experimental studies.

The following three cases are considered to show the effectiveness of the proposed controller under steady-state operation.

- 1) Case-B1: Balanced reference currents $(i_a^* = i_b^* = i_c^* = 10 \text{ A})$ and balanced loads $(R_a = R_b = R_c = 7.5 \Omega)$.
- 2) Case-B2: Balanced reference currents $(i_a^* = i_b^* = i_c^* = 10 \text{ A})$ and unbalanced loads $(R_a = 5 \Omega, R_b = R_c = 7.5 \Omega)$.
- 3) Case-B3: Unbalanced reference currents ($i_a^*=10~{\rm A},$ $i_b^*=5~{\rm A},$ $i_c^*=5~{\rm A})$ and balanced loads ($R_a=R_b=R_c=10~\Omega$).

Steady-state experimental results of these cases are shown in Fig. 7(a)–(c). All experimental results show that the output currents (i_a, i_b, i_c) and the capacitor voltage (V_{C1}) track their references $(i_a^*, i_b^*, i_c^*, V_{C1}^*)$ with high accuracy while the dc-link voltage (V_{PN}) is kept constant. The neutral current, which is the sum of the three-phase load currents, is zero in cases of balanced reference current [see Fig. 7(a) and (b)]. On the other hand, the neutral current flows through the fourth leg of the inverter in case of the unbalanced reference current [see Fig. 7(c)]. It can be observed that the inductor current (i_{L1}) remains continuous, which significantly reduce the input stress. It is important to note that double-line frequency $(2*f_o)$ ripple exist on the qZS inductor current, capacitor voltages, and dclink voltage due to the unbalanced currents. However, it can be observed from Fig. 7(b) and (c) that these ripple are very low and these are dependent on the design of qZS network.

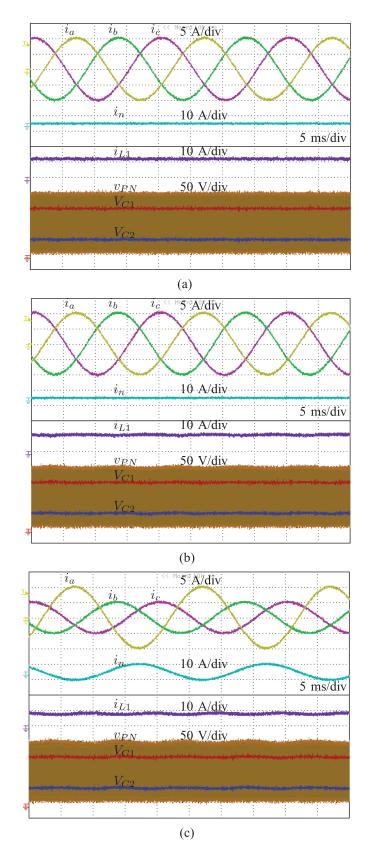


Fig. 7. Experimental results of steady-state analysis with (a) balanced reference currents and balanced loads; (b) balanced reference currents and unbalanced loads; and (c) unbalanced reference currents and balanced loads.

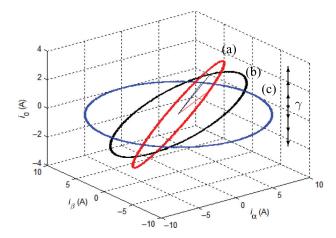


Fig. 8. Trajectories of output current under various reference currents (a) i_a =10, i_b =0 A, i_c =10 A; (b) i_a =10, i_b =5 A, i_c =5 A; and (c) i_a = i_b = i_c =10 A.

The simulation result of the load currents trajectories under various reference values is shown in Fig. 8. The blue trace (c) is balanced current condition, while the black (b) and red (a) are unbalanced. The trajectory under balanced current condition shows a circle shape and the zero-sequence current is zero. On the other hand, the trajectories under unbalanced current condition show an oval shape and the zero-sequence current travels alongside the γ -axis.

C. Transient-State Analysis

The simulation results of transient-state analysis with balanced and unbalanced reference currents are shown in Fig. 9(a) and (b), respectively. The reference output currents step from 5 to 10 A are shown in Fig. 9(a). For this test, reference loads $(R_a=R_b=R_c=6\,\Omega)$ are balanced. It can be seen that the output currents track to the references with fast rise time and no overshoot. The qZS network voltage $(v_{\rm PN})$ is also kept constant by the proposed controller at the current step-up instant.

In Fig. 9(b), the results are presented with unbalanced reference current step change and balanced loads ($R_a=R_b=R_c=6\,\Omega$). For this test, all reference output currents are set to 5 A at the beginning. Then, reference currents are set to $i_a^*=7\,\mathrm{A}$, $i_b^*=10\,\mathrm{A}$, and $i_c^*=12\,\mathrm{A}$. Results of this test show that the proposed controller handles each phase current independently and the output currents (i_a,i_b,i_c) and the capacitor voltage (V_{C1}) track their references ($i_a^*,i_b^*,i_c^*,V_{C1}^*$) with high accuracy while the dc-link voltage (V_{PN}) is kept constant. However, the double-line frequency (2^*f_o) ripple exist on the qZS network due to unbalanced current.

The experimental results with the same operating conditions are shown in Fig. 10(a) and (b), respectively, which totally agree with the simulation results. It can be clearly seen from the results that the transient time is very short, and there is no overshoot. Furthermore, the output currents are controlled independently by the proposed controller.

D. Analysis of Fault-Tolerant Capability

The proposed system is also tested for a fault condition, which may occur during the operation of the three-phase

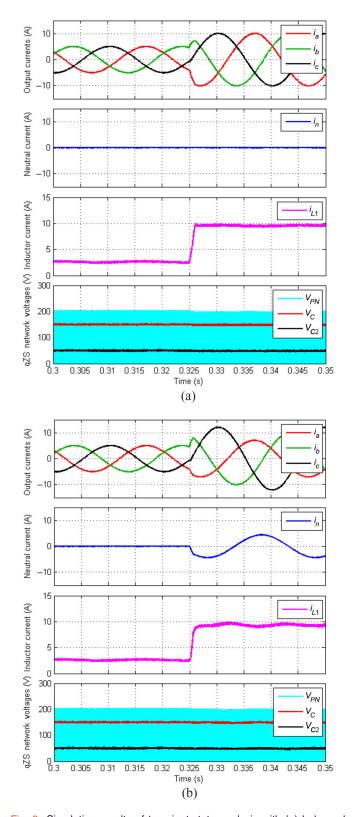


Fig. 9. Simulation results of transient-state analysis with (a) balanced reference currents and balanced loads and (b) unbalanced reference currents and balanced loads.

inverters. To do that, one-phase is made an open circuit and the corresponding reference current (i_b^*) is set to 0 A. The transient-state experimental results are shown in Fig. 11(a). It is clear that even with single-phase open-circuit fault condition, the

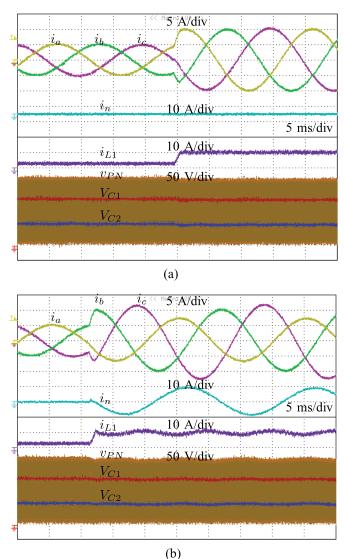


Fig. 10. Experimental results of transient-state analysis with (a) balanced reference currents and balanced loads and (b) unbalanced reference currents and balanced loads.

output currents are controlled independently by the proposed controller and the circulating current flows through the fourth leg of the inverter. Although there is a single-phase open-circuit fault, inverter can supply the loads of other two phases with low (2.8%) total harmonic distortion (THD), as shown in Fig. 12(a).

To compare fault-tolerant capability of the proposed system with a traditional MPC qZS three-leg inverter, the system is tested under a single-phase open-circuit fault condition. In this test, the neutral point of the load is connected to the star point of the secondary side of the Δ/Y transformer, which is connected to the output of qZSI, to observe the circulating current. The "b" phase is open-circuited and the corresponding reference current (i_b^*) is set to 0 A similar to previous case in Fig. 11(a). Experimental results of this test are shown in Fig. 11(b). The stability of the qZS network deteriorated after single-phase fault. The inductor current is discontinuous that increases the input stress, and the output current waveforms affected from the fault. Furthermore, the output current of THD is higher than previous case, as shown in Fig. 12(b). As a result of this test, the

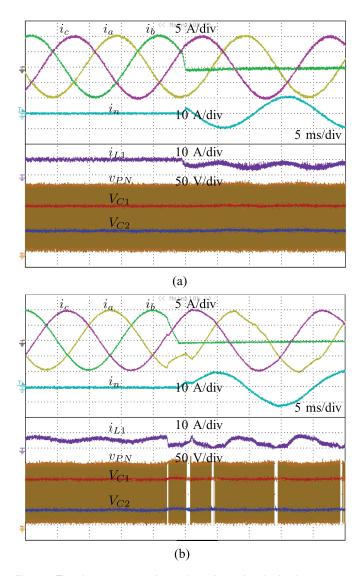


Fig. 11. Transient-state experimental results under single-phase opencircuit fault. (a) Proposed qZS four-leg inverter. (b) Traditional qZS threeleg inverter with MPC control.

proposed qZS four-leg inverter offers much better fault-tolerant capability than traditional three-phase inverter.

E. Analysis of Symmetrical Components

To analyze the symmetrical components (zero, positive, and negative sequences) of the three-phase current signals under unbalanced conditions, Fortescue method is used [37]. The level of unbalance is also described by the negative sequence current unbalance factor (ρ_i) , which is given as the modulus of the ratio of negative to positive sequence currents [same for the negative sequence voltage unbalance factor (ρ_v)] [38]

$$\rho_i = \frac{i_n}{i_p} * 100 \,(\%) \tag{29}$$

where i_p and i_n are the positive- and negative-sequence component, respectively. According to the Fortescue method and definition given in (29), Table II shows some of the case studies

HARMONICS TABLE					
		© 0:00:20	3	Up ⊡-Œ	
Amp	A	В	C	N	
THD%e	2.8	0.2	2.8	2.7	
H3%r	1.4	0.1	1.3	1.2	
H5%r	1.7	0.2	1.6	1.6	
H7%r	0.8	0.1	0.8	0.8	
H9%r	0.1	0.2	0.1	0.2	
H11%r	0.2	0.3	0.4	0.4	
H13%r	0.2	0.1	0.1	0.1	
H15%r	0.1	0.1	0.1	0.1	
03/05/15 15:34:55 230V 50Hz 3Ø WYE EN50160					
PREU	BACK	NEXT	PRINT	USE []	
		(a)			

HARMONICS TABLE					
_		♦ 0:00:38		:D-⊡ qU	
Amp	A	В	C	N	
THD%r	4.3	0.3	8.7	3.7	
Н3%г	3.4	0.2	6.3	1.2	
H5%r	2.7	0.1	4.6	1.6	
H7%r	1.8	0.1	2.8	0.8	
H9%r	1.1	0.2	1.8	0.6	
H11%r	0.8	9.0	1.4	0.4	
H13%r	9.0	0.1	1.2	0.1	
H15%r	0.1	0.1	1.1	0.1	
15/10/15 13:54:55 230V 50Hz 3Ø WYE EN50160					
PREV	BACK	NEXT	PRINT	USE 🗀	
		(b)			

Fig. 12. THD under single-phase open-circuit fault. (a) Proposed qZS four-leg inverter. (b) Traditional qZS three-leg inverter with MPC control.

TABLE II
SYMMETRICAL COMPONENTS AND UNBALANCE FACTOR

Case studies	i_0	i_p	i_n	ρ_i (%)
Fig. 7 (a):				
$i_a = i_b = i_c = 10 \text{ A}$	0 A	10 A	0 A	0
Fig. 7 (c):				
$i_a = 10 \text{ A}, i_b = i_c = 5 \text{ A}$	1.67 A	6.67 A	1.67 A	25
Fig. 8 (a):				
$i_a = i_c = 10 \text{ A}, i_b = 0 \text{ A}$	3.33 A	6.67 A	3.33 A	50
Fig. 10 (b):				
$i_a = 7 \text{ A}, i_b = 10 \text{ A}, i_c = 12 \text{ A}$	1.45 A	9.67 A	1.45 A	15

and their symmetrical components, and the negative sequence current unbalance factor. Phase angles of the currents are $\theta_a=0^\circ$, $\theta_b=-120^\circ$, and $\theta_c=-240^\circ$.

V. CONCLUSION

This paper has proposed an MPC scheme for qZS three-phase four-leg inverter. The main aim of this paper is to achieve single-stage power converter topology for renewable energy-based power generation systems under balanced and unbalanced conditions with high control capability. To do that, qZS three-phase four-leg inverter topology was proposed in this study. To improve control capability of the controller, the MPC scheme was employed in the controller stage. Simulation and experimental studies were performed to verify the performance of the proposed inverter topology and its control strategy. The results show that the proposed technique not only has an excellent steady-state and transient performances, but also it is robust against fault conditions.

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